entirely within a prescribed region of one surface of said semiconductor thin film through a gate insulating film,

wherein said semiconductor thin film is formed by forming a 30 to 80 nm layer of non-single crystal silicon on said other substrate, and irradiating said prescribed region of said substrate in its entirety once or more with a pulse of laser light having a constant cross sectional area and an emission time width of 50 ns or more under conditions in that said other substrate is cooled to a temperature lower than room temperature, so as to convert said non-single crystal silicon contained in an irradiated area corresponding to said cross sectional area to a polycrystalline silicon at a time.

REMARKS

This is a full and timely response to the Official Action mailed April 8, 2002. A petition for a one-month extension of time and authorization to pay the requisite fee are filed herewith. Reexamination and reconsideration in light of the above amendments and the following remarks are courteously requested.

In the outstanding Office Action, the Examiner newly rejected claims 11, 39, 53, 63, and 73 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,017,779 ("Miyasaka"). The Examiner also rejected remaining claims 12,

18, 28, 40, 54, 63, and 73 under 35 U.S.C. § 103(a) as being unpatentable over Miyasaka in view of 5,798,744 ("Tanaka"). These rejections are respectfully traversed in light of the present amendment.

The claims that are pending for the Examiner's consideration in this application are apparatus claims that are directed to the thin film semiconductor devices that result from an inventive method. It is recognized that process limitations in product claims are not given any patentable weight **unless** they ascribe a structural feature to the resulting semiconductor chip. Therefore, the following discussion establishes how the process steps in the present claims do in fact ascribe a structural feature to the semiconductors made thereby, which distinguish the semiconductors from those of the prior art.

Each of independent claims 11 to 12, and 17 to 18 recites that a thin film semiconductor is formed by irradiating an amorphous semiconductor substrate with an energy beam that has an adjusted cross sectional shape so that a region of the substrate is irradiated with a single shot, so that a resultant polycrystalline silicon substrate is uniform in its crystallinity. Throughout the present specification (i.e., page 51, lines 7 to 12) it is repeatedly taught that by irradiating the entirety of the unit size of the thin film semiconductor device that the crystallization of the silicon

film is made continuous, avoiding the formation of borders in the crystallized silicon. The specification also teaches that such borders are the product of conventional crystallization processes that involve the piecemeal irradiation of several adjacent regions of the unit size of the semiconductor device. The borders in the conventional process are the result of slight overlapping of regions that are separately irradiated. Consequently, the single shot irradiation process of the present invention does ascribe a structural limitation to the resultant thin film semiconductor that sets the structure apart from thin film semiconductors that are formed by irradiation of several adjacent regions in a unit area.

The newly cited Miyasaka patent appears to disclose the very type of conventional process discussed in the background section of the present application, and briefly described above. As disclosed at column 36, lines 28 to 48, Miyasaka teaches that 8 mm x 8 mm regions of a unit area of amorphous silicon are individually irradiated, with overlapping areas of 2mm x 2 mm due to the movement of the movement of the substrate 4 mm in both the horizontal and vertical directions between each irradiation. In light of the present teachings of the present application, and to further distinguish the invention from the prior art, claims 11 to 12, and 17 to 18 are amended to recite:

"a gate electrode accumulated on a region of said semiconductor thin film through said gate insulating thin film, ...

a cross sectional shape of said energy beam is adjusted with respect to said region to irradiate said region in its entirety at a time by a single shot irradiation, so that characteristics of said thin film transistor are made uniform."

In contrast, Miyasaka's process would result in the very border regions that the present invention overcomes by use of the single shot radiation. The remaining claims are similarly amended to overcome the remaining rejections.

"A claim is anticipated [under 35 U.S.C. § 102] only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). See M.P.E.P. § 2131. Likewise, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." M.P.E.P. § 2143.03. Accord. M.P.E.P. § 706.02(j). Because the above-discussed features of the claims are neither taught nor suggested by the prior art of record, it is respectfully

requested that the rejections of the claims be withdrawn.

For the foregoing reasons, all the claims now pending in the present application are believed to be clearly patentable over the prior art of record. Accordingly, favorable reconsideration of the claims in light of the above remarks is courteously solicited. If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone the undersigned attorney at the below-listed number.

Respectfully submitted,

DATE: August 8, 2002

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